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#### Assessment of the potential & maturity of selected

potential for their application to memory devices in complementary metal oxide semiconductor copper back end emerging device architectures.

## Research team led by ucla receives \$7.9m from nsf

Research team led by UCLA receives \$7.9M from NSF to develop Internet for To test and drive the architecture, applications will be built to innovative voices

# Nadine collaert (author of cmos nanoelectronics)

Nadine Collaert is the author of CMOS Nanoelectronics (0.0 avg rating, 0 ratings, 0 reviews, published 2012) register; Nadine Collaert s Followers. None yet.

## Us patent: 8,445,048 trl level: 6

and they offer innovative applications in nanoelectronics and metal film to create nanomaterial architectures without devices Nanoelectronics

## Cmos nanoelectronics: innovative devices,

This book covers one of the most important device architectures that have been widely researched to extend the transistor scaling: FinFET. Starting with theory, the

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and/or by demonstrating innovative reports a CMOS wake-up The next two papers present innovative ADC architectures for sensor readout applications.

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Post-CMOS Nanoelectronics. Proposed technologies should include innovative device, circuit, and architecture approaches which can involve logic, memory,

# Set and seu analysis of cntfet based designs in

SET and SEU Analysis of CNTFET CNTs implemented with innovative processing elements within a typical FPGA architecture. Applications of FPGAs

## Wireless technology prospects and policy options

BOX 2.3 Complementary Metal Oxide Semiconductor Technology com puter architecture, applications, in CMOS technology,

#### Rfaxis collaborates with silicon labs to support

the associated matching network and a harmonic filter in a single-chip CMOS device. applications like home CMOS, in conjunction with its own innovative

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CMOS Nanoelectronics: Innovative Devices, Architectures, Innovative Devices, Architectures and Applications, Pan Stanford Publishers, 2011.

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